Department of Electrical and Computer Engineering
The University of Texas at Austin

ECE 382N, Spring 2008
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"Compile-time" Course Outline
January 14, 2008

January 14: **First class meeting**. Introduction to the course, administrative details. Focus of the course: Principles and Tradeoffs. Levels of transformation, Instruction supply, data supply, processing.

January 15: **First discussion session**. Orientation. Introduction to the CAD tools we will be using in the course.

January 16: Basic concepts in architecture and microarchitecture. Critical path, Bread and Butter Design, Compile time vs. Run time. Partitioning, Timing, Pipelining. Data Path, state machine, microsequencer, microinstruction definition, and microcode. Microprogramming (horizontal, vertical, two-level, dynamic microprogramming, bit steering). Pipelining and pipelined control.

January 17, 18: Extra discussion sessions, for those who feel they need it.

January 21: No class, Martin Luther King Day

January 22: Discussion session. Review of the use of the CAD tools on the logic design of a simple ALU.

Problem Set 1a due at the start of discussion session.

January 23: The x86 ISA in the context of ISA tradeoffs. Some implementation issues.

January 24, 25: Extra discussion sessions, for those who feel they need it.

January 28: ISA tradeoffs, continued.

January 29: Discussion session. CAD tools, continued.

Problem Set 1b due at the start of discussion session.

January 30: The basic Superscalar, out-of-order execution model. Effective use of long pipelines without blocking. The structure of a modern pipeline. Functions at each stage.

February 4: Run-time optimizations: Trace Cache, Runahead, etc.

February 5: Discussion session

February 6: Compile time optimizations: The Block-structured ISA, Predication, leading to wish branches, Braids, etc. Preview to the future: multiple levels of cache, fast track/slow track.

February 11: Simultaneous Multithreading and SSMT.

Problem Set 2 due at the start of class.

February 12: Discussion session.

February 13: Guest lecture: Professor Mateo Valero Cortes

February 18: Discussion session.
February 19: Discussion session.
February 20: Discussion session.

February 25: Branch Prediction.

Problem Set 4 due at the start of class.

February 26: Discussion session.

February 27: Branch Prediction, continued. Indirect Jumps, Perceptron Predictors, O-GEHL.

March 3,4,5: Individual group meetings to define group implementations.

March 6,7: First Design Review in 541a ENS, by appointment.

March 10 through 14: Spring break, no class.

March 17: The off-chip memory bottleneck.

March 18: Discussion session, as needed.

March 19: Review, or catch up, as needed.

March 24: **Written exam, in class**.

March 25: Discussion session, as needed.

March 26: Measurement methodology and abuses.

March 31: RISC, a Retrospective.

April 1: Discussion session, as needed.

April 2: Multiple processor issues. interconnect, steering, memory consistency, transactional memory.

April 7: Multiple processors: Cache Coherency.

April 8: Discussion session, as needed.

April 9: Alternative approaches to Concurrency

April 14: Alternative approaches to Concurrency, continued.

April 15: Discussion session, as needed.

April 16: Case Studies: Pentium M, Niagara, Cell, Power 6, GPGPUs.

April 17,18: Additional design reviews, as needed.

April 21: Case Studies (continued).

April 22: Discussion session, as needed.

April 23: Guest lecture from local industry (to be determined).

Oral exams (Exam 2) will be given in 541a ENS on April 24,25.

April 28: Microarchitecture of the microprocessor of the year 2016.

April 29: Discusssion session, as needed.

April 30: Last class meeting. Review of the course.

Final project design reviews in 541a, May 1,2 by appointment.

May 9: Final project report due in 541a, 10pm.

Note: there will be no final exam in this course.