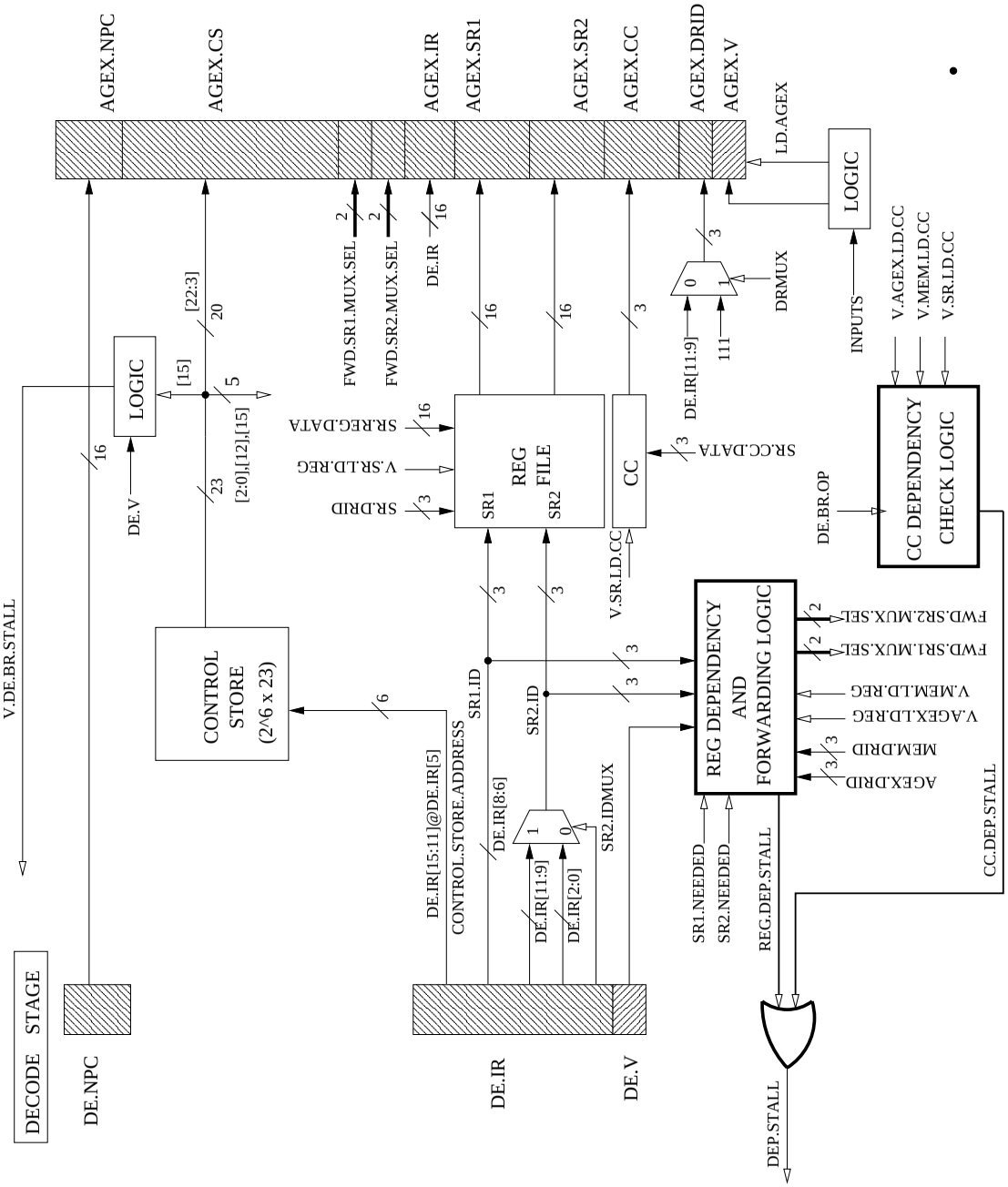


Fig.3 Decode Stage (DE–Stage)

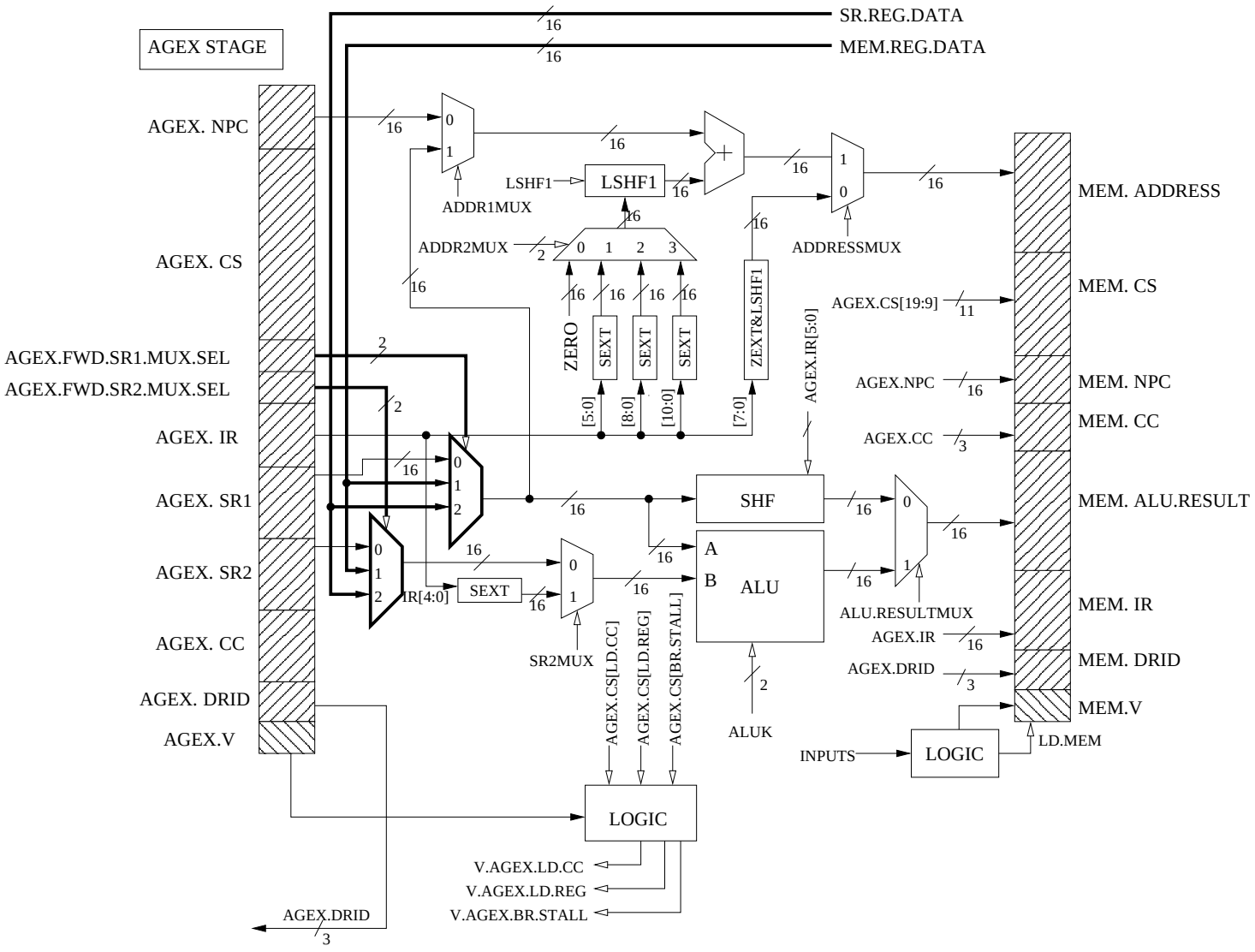


Fig.4 Address Generation Stage (AGEX−Stage)

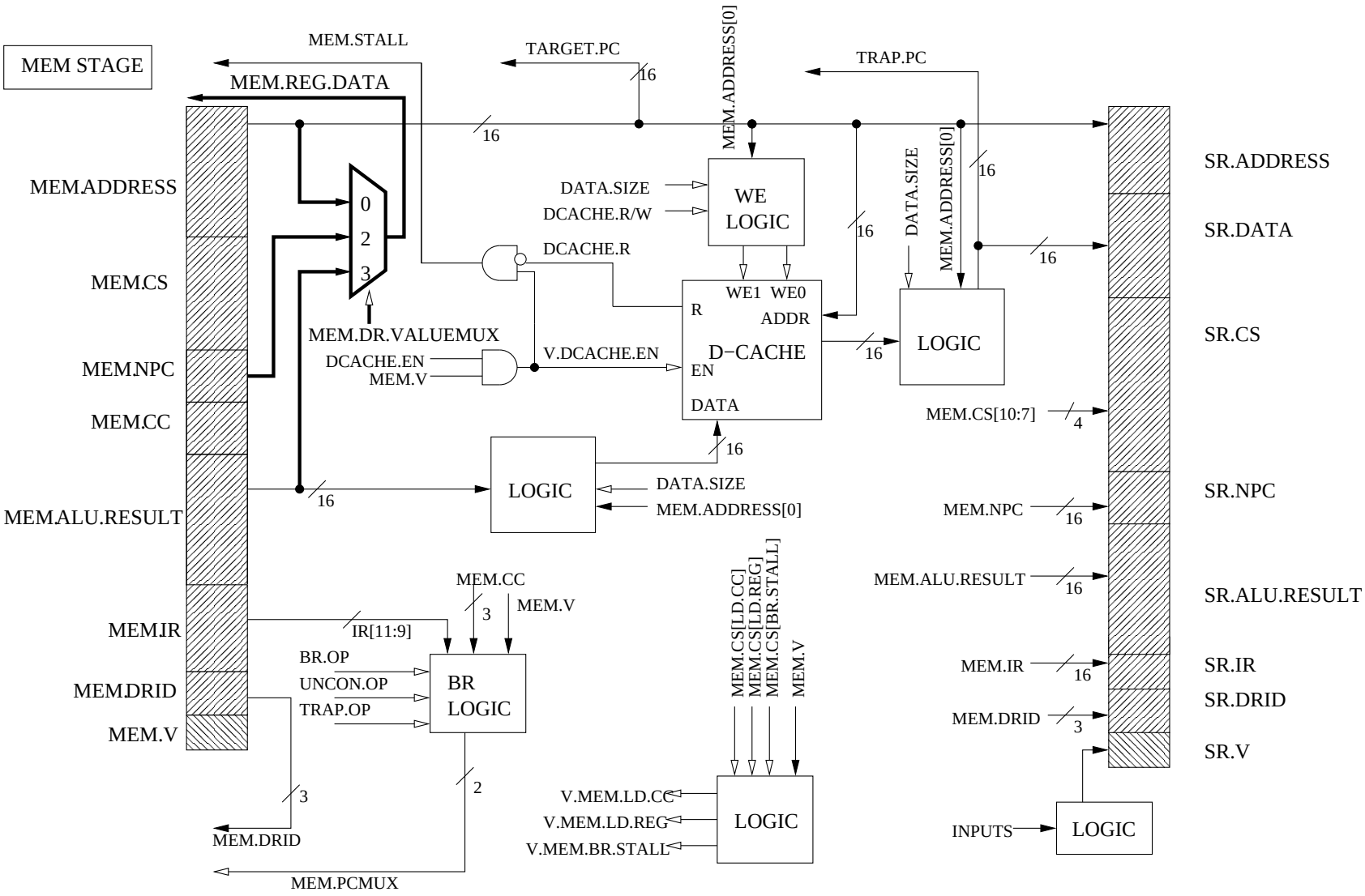


Fig. 5 Memory Stage (MEM−Stage)

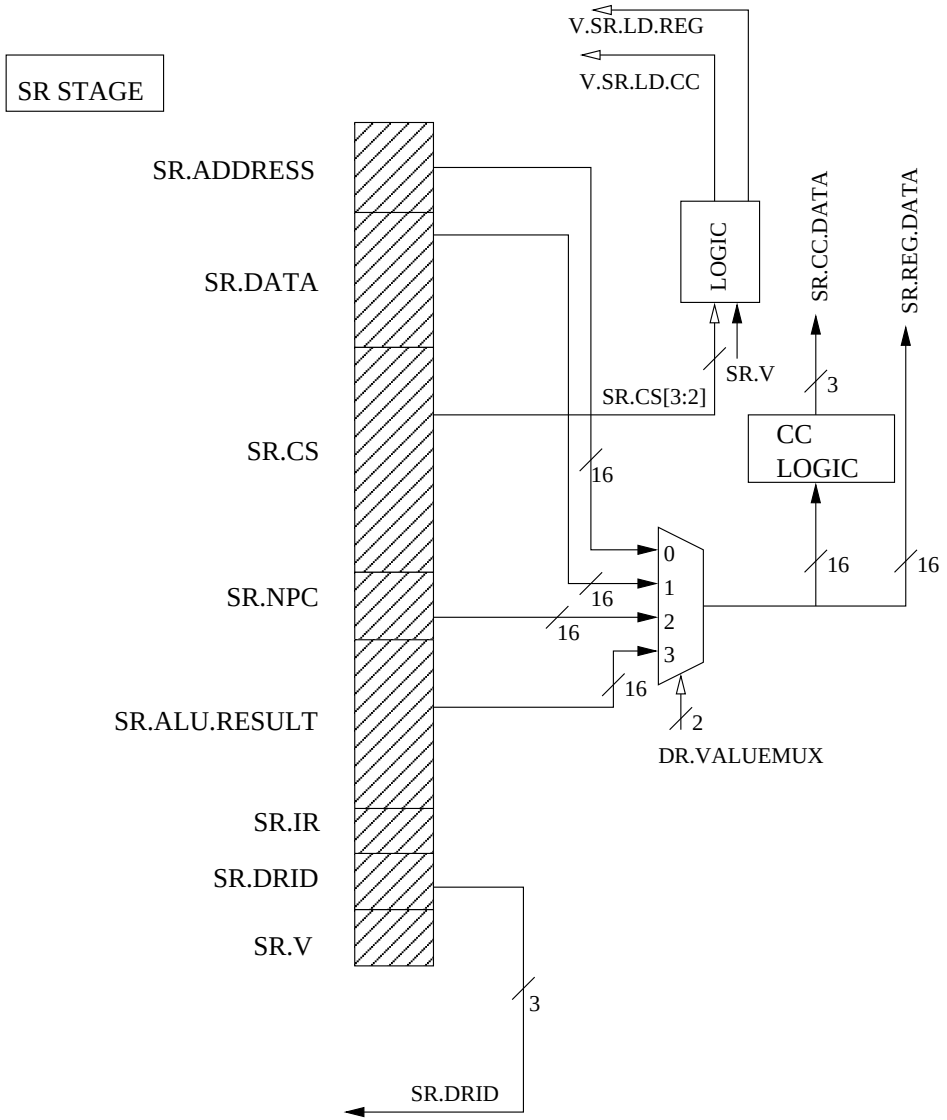


Fig.6 Store Result Stage (SR−Stage)