Department of Electrical and Computer Engineering
The University of Texas at Austin

EE 360N, Fall 2003
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Exam 1, March 5, 2003

Name:_____

Problem 1 (20 points):_____

Problem 2 (20 points):_____

Problem 3 (20 points):_____

Problem 4 (20 points):_____

Problem 5 (20 points):_____

Total (100 points):_____

Note: Please be sure that your answers to all questions (and all supporting work that is required) are contained in the space provided.

Note: Please be sure your name is recorded on each sheet of the exam.

GOOD LUCK!

Name:_____

Problem 1 (20 points):

Part a (5 points): All of the following are important considerations that every manufacturer deals with in the design of its next microprocessor. Circle all those that are provided to increase performance of the executing program:

compatibility

unaligned accesses

memory interleaving

a TLB

virtual memory

Part b (5 points): A process is running at priority k, when a page fault occurs.
The page fault should be serviced at priority:

$>$k,

$=$k,

$<$k.

Circle one. Explain in ten words or less.

Part c (5 points): Two structures already discussed in class that can be classified as content addressable memories are

and

Part d (5 points): Since the microarchitect is able to use all the internal structures of the microarchitecture to his/her convenience, what is the first thing the hardware has to do in dealing with an exception or interrupt? Ten words or less, please.

Name:_____

Problem 2 (20 points):

A 2-way set associative write back cache with perfect LRU replacement requires 15 x 2^9 bits of storage to implement its tag store. The cache is virtually indexed, physically tagged. The virtual address space is one megabyte; page size is 2 KB; cache block size is 8 bytes.

Part a (10 points) What is the size of the data store of the cache (CacheD) in bytes.

Part b (5 points) How many bits of the virtual index come from the virtual page number?

Part c (5 points) What is the physical address space of this memory system?

Name:_____

Problem 3 (20 points):

We wish to add virtual memory to the LC-3b. What we have been calling addresses thus far will now be called virtual addresses. That is, VA space is 2^{16} bytes. We wish to specify our memory management system in a way similar to the VAX, which we have studied. However, we will only designate 1/8 of the VA space as system space, specifically the last 1/8 of the VA space (locations xE000 to xFFFF). Assume PA space is 2^{10} bytes, and page size is 2^6 bytes.

Page tables are formed in the same way we did for the VAX, with each PTE containing 3 access control bits, a reference bit (unlike the VAX), and other bits that make sense.

The P0BR is xE040.
The SBR is 0x020.

Part a (3 points) What is the appropriate size for a PTE?

Part b (5 points) What is the maximum size of the system page table?

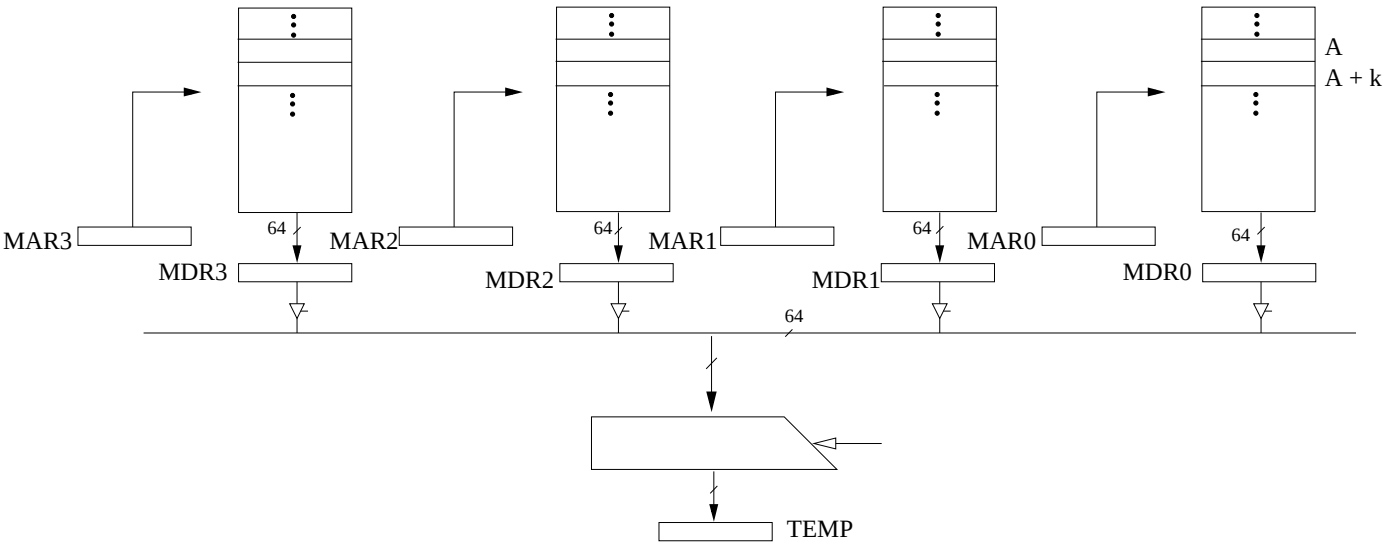
Part c (6 points) The VA of Y is x0082. What is the VA of the PTE of the page containing Y?

Part d (6 points) The VA of Z is xE100. What is the PA of the PTE of the page containing Z?

Name:_____

Problem 4 (20 points):

A four-way interleaved, byte-addressable memory is shown in the figure. We can load one MAR each successive cycle if necessary. It takes ten cycles after the MAR is loaded, to load the corresponding MDR with the contents of the memory locations in its respective memory array. It takes an additional cycle to gate MDR onto the bus and load its contents into TEMP. The processor supports unaligned memory accesses. LDBIG loads 64 bits from memory into a register.



Part a (3 points) Note the address labeled A+k. What is k?

Part b (3 points) How many LD_ENABLE signals are required for TEMP?

Part c (4 points) Consider LDBIG R3, B, where B is a multiple of 8. How many cycles are required to get the contents of B into TEMP, after the appropriate MAR is loaded with B.

Name:_____

Problem 4 continued:

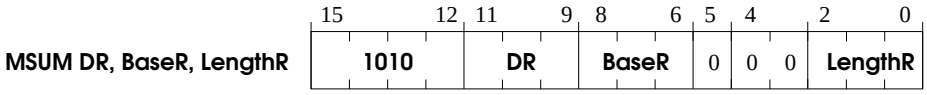
Part d (5 points) Redo Part c if B is decimal 8002.

Part e (5 points) In Part d, which LD_ENABLE signals of TEMP are asserted in the cycle where TEMP is loaded with its final value (the contents of B).

Name:_____

Problem 5 (20 points):

We wish to add to the LC-3b the new instruction MSUM, which adds the contents of k consecutive memory locations, and stores the result in one of the general purpose registers. The condition codes will be set according to whether the result is negative, zero, or positive. We will use the unused opcode 1010 for this purpose. The format of the instruction will be



where the address of the first location to be added is in BaseR, and the number of locations to be added is in LengthR.

If LengthR is initially 0, MSUM stores 0 in DR.

There is no requirement that the contents of BaseR or LengthR remain unchanged at the end of this instruction's execution.

Example:
After the instruction MSUM R1,R2,R3 is executed, where R2 contains x4000, R3 contains #5, and memory is as shown below, R1 will contain the value #8, and condition P will be set.

x4000	1
x4001	2
x4002	0
x4003	3
x4004	2

Name:_____

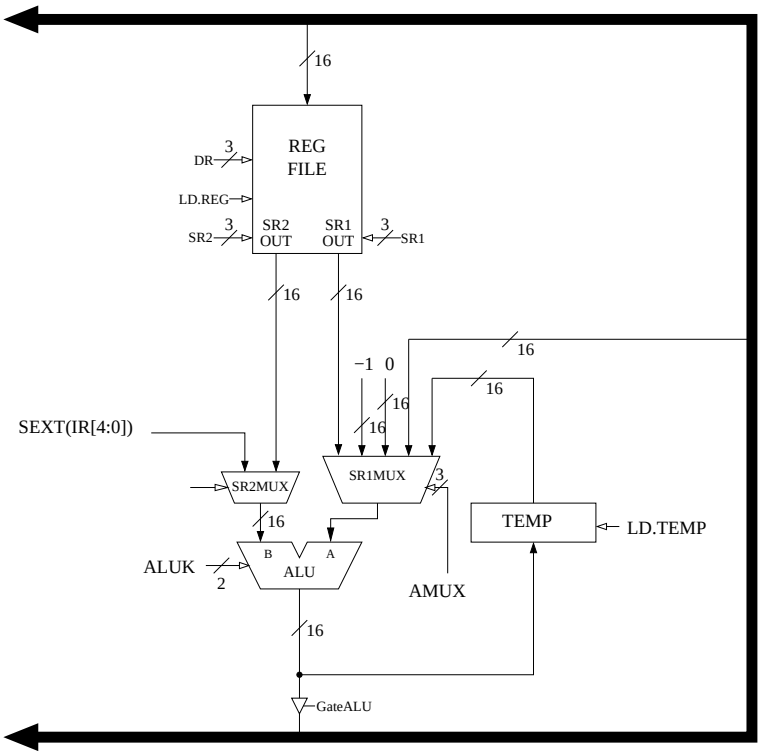
Problem 5 continued:

To implement MSUM, we have chosen to add the following to the LC-3b data path:

1. A new TEMP register, which is sourced from the output of the ALU.
(This requires a new control signal, LD_TEMP)

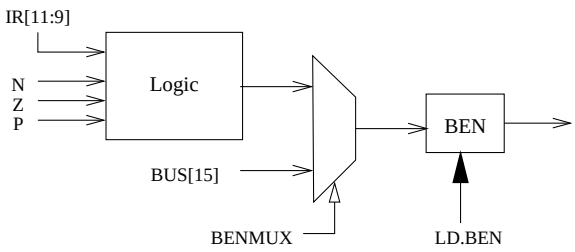
2. A five-input MUX to the A input of the ALU.
(This requires a new control field, AMUX, specified as follows:

SR1/000, the SR1 source from the original data path,
MINUS1/001, a constant -1
ZERO/010, a constant 0
BUS/011, the contents on the bus
TEMP/100, The contents of the new TEMP register



We have also added a BENMUX at the input of the BEN register, as shown.
This requires a new control signal, BENMUX, specified as follows:

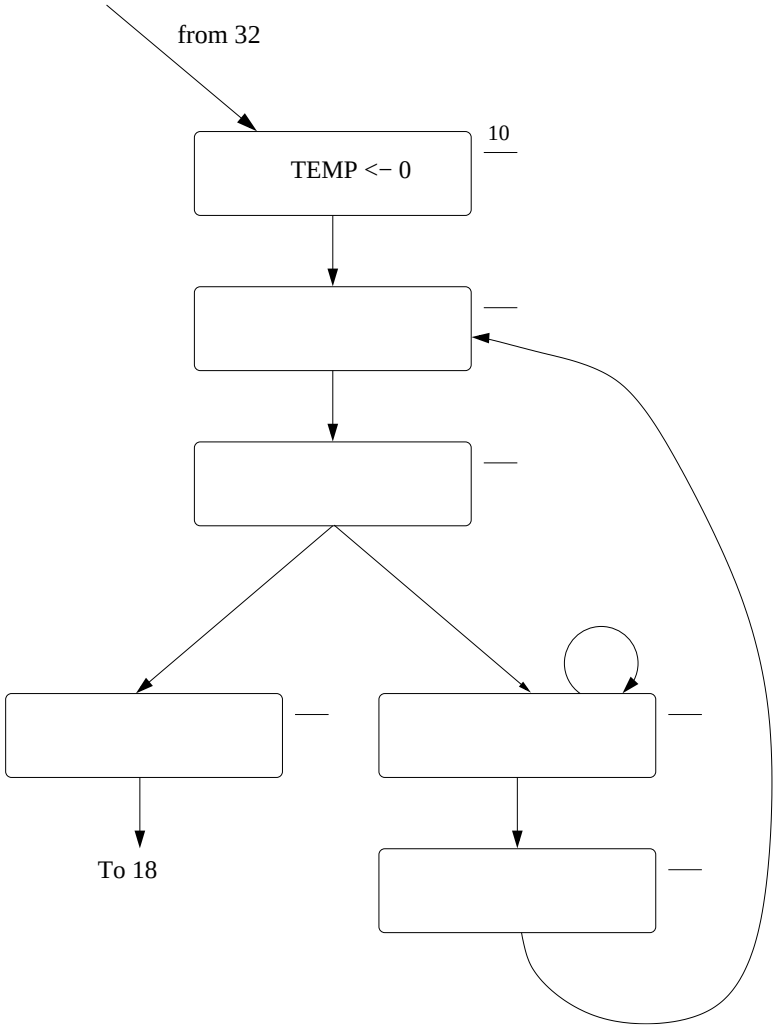
Logic/0
BUS[15]/1



Name:_____

Problem 5 continued:

Part a. (12 points): We have provided the skeleton of the augmented LC-3b state machine for you to implement MSUM. Using the notation we have adopted for the LC-3b, show what happens in every state. Specify the assignment (i.e, the state number) of each state you use. The five states should be selected from the set 56, 58, 60, 61, 63. Note that state 10, the first state after decode, has both been assigned its state number (i.e., ”10”) and also has been filled in.



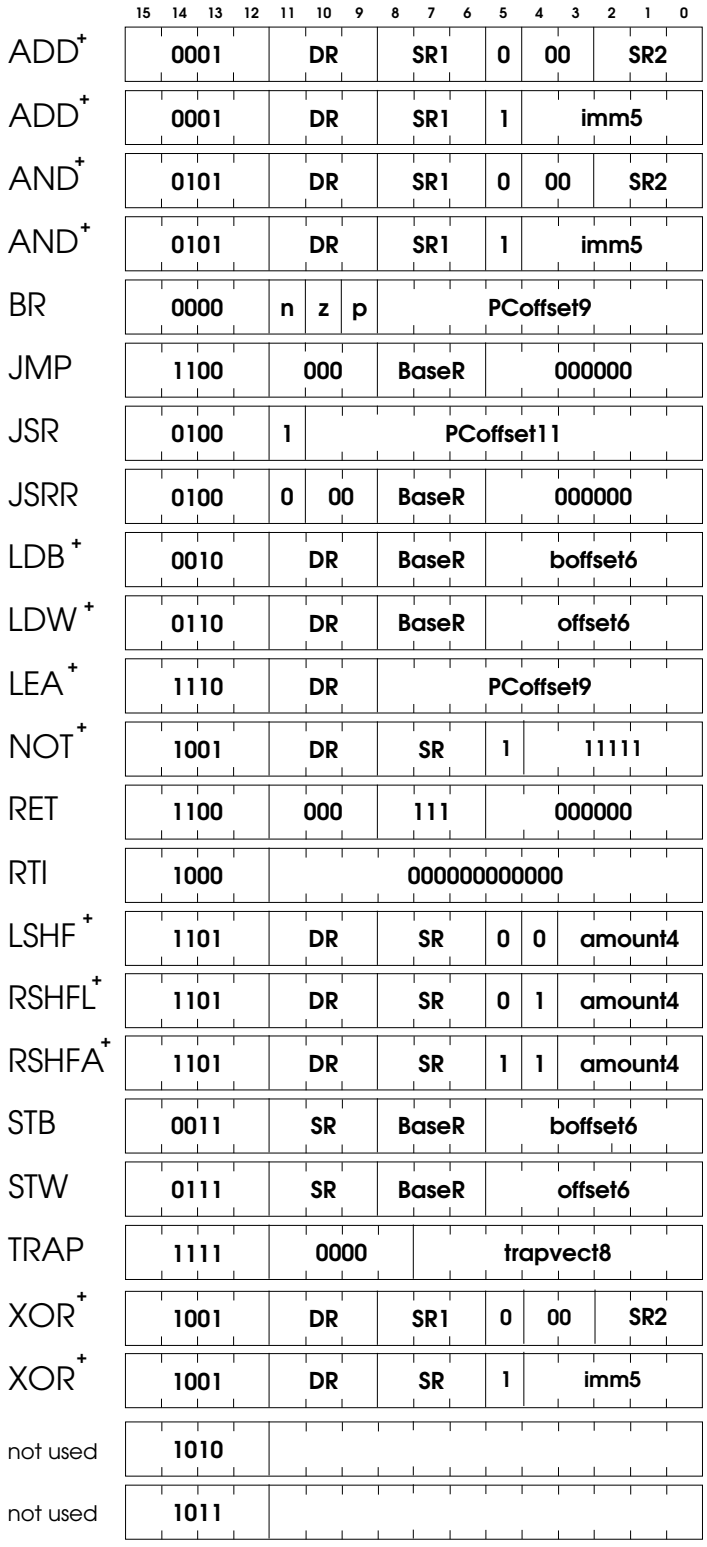
Name:_____

Problem 5 continued:

Part b. (8 points): Specify the control signals required (for both data path control and microsequencer control) to implement each state. Note that we have added control signals corresponding to our changes in the data path.

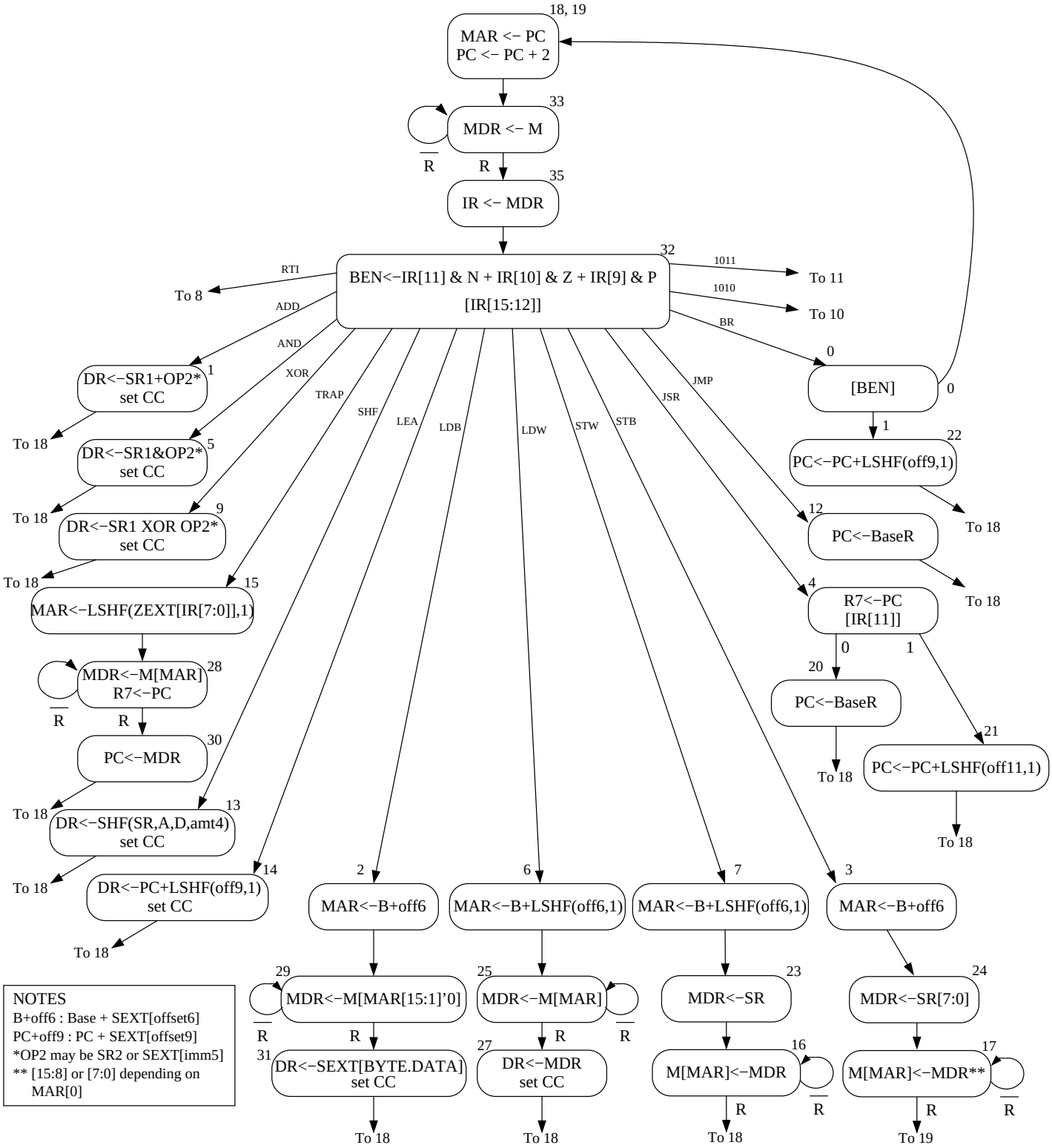
	IRD	Cond	J
10			
56			
58			
60			
61			
63			

	LD.MAR	LD.MDR	LD.IR	LD.BEN	LD.REG	LD.CC	LD.PC	GatePC	GateMDR	GateALU	GateMARMUX	PCMUX	DRMUX	SR1MUX	ADDR1MUX	ADDR2MUX	MARMUX	ALUK	MIO.EN	R.W	LD.TEMP	BENMUX	AMUX
10																							
56																							
58																							
60																							
61																							
63																							

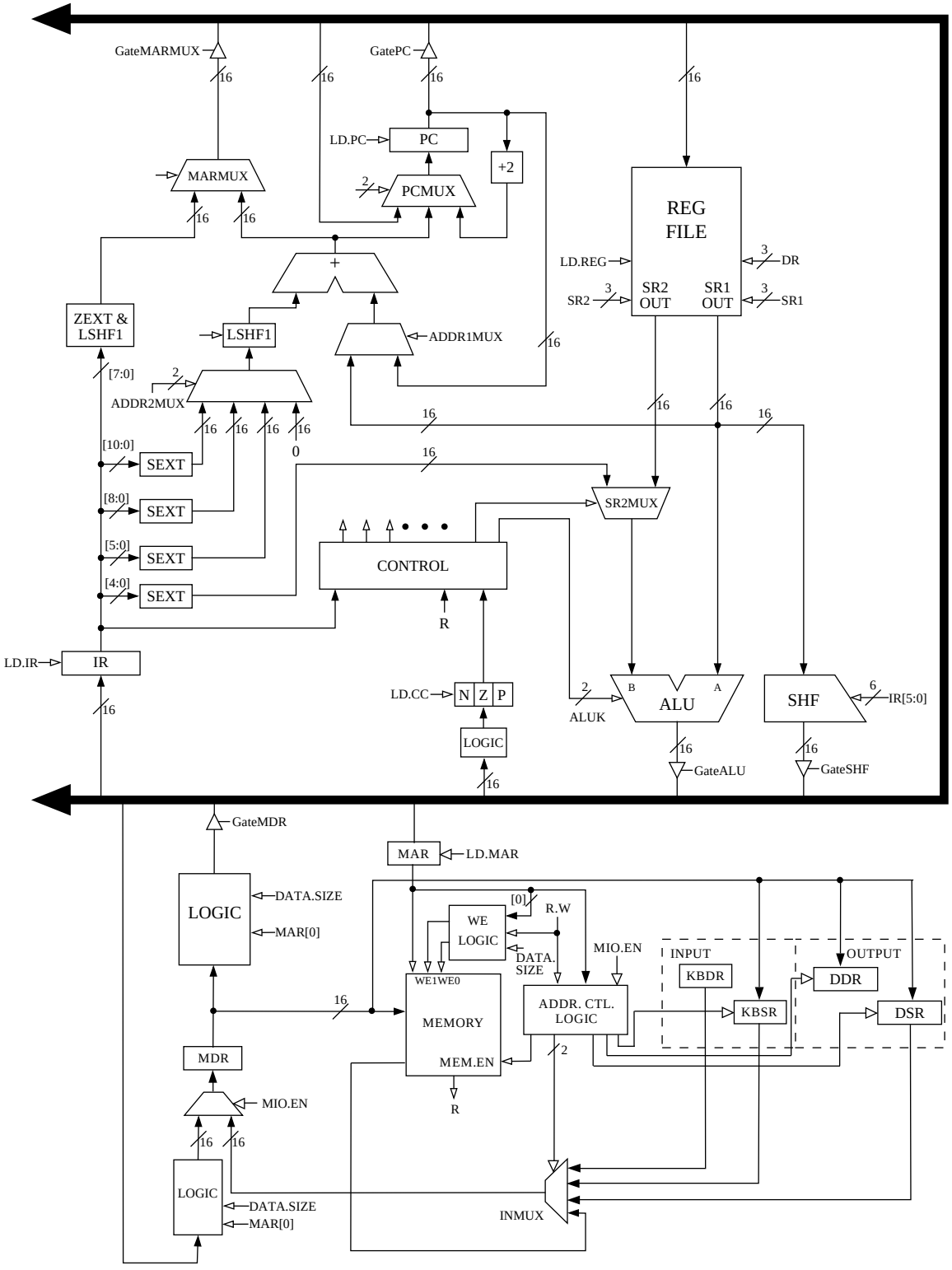


+ indicates instructions that modify condition codes.

A state machine for the LC-3b (from Appendix C)



The LC-3b datapath (from Appendix C)



The Microsequencer of the LC-3b base machine (from Appendix C)